LED Driver Achieves Electrolytic Capacitor-Less and Flicker-Free Operation with an Energy Buffer Unit

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***Abstract*—In this paper, a cycle-by-cycle energy buffering LED driver has been proposed to achieve electrolytic capacitor-less flicker-free operation. An energy buffering unit (EBU), with high voltage film capacitors being the energy storage device, is introduced in the design to buffer imbalanced energy in every switching cycle. The switching current can be controlled to meet high power factor correction and deliver DC LED output current at the same time. Compared to previous electrolytic capacitor-less designs, it can reduce circulating power and, therefore, also reduce power conversion loss. A 15W experimental prototype had been built and tested to verify the proposed LED driving method.**

I INTRODUCTION

LED lighting gains more and more popularity owing to its high efficacy, long lifespan, and environment-friendly operation. It is replacing fluorescent lighting and becoming major artificial lighting sources in various applications. Although having inherent advantages over fluorescent, more technical challenges need to be overcome to properly use them, particularly with the AC powered LED driver, in which notorious twice-line-frequency flicker often occurs. The key to gain full benefits of LED lighting lies in LED driver designs.

EnergyStar requires power factor correction (PFC) implemented with higher than 5W lighting devices. Power factor should be higher than 0.9 for commercial usages and 0.7 for residential usages [1], which results in a time-varying input power with a twice-line-frequency ripple and creates twice-line frequency lighting flicker in a single-stage LED driver. Twice-line-frequency flicker rises health-related concerns. Although it is usually not visible, it can be picked up by retina that leads to visual fatigue and other problems [2]. Conventional two-stage LED driver can naturally achieve flicker-free LED driving. The additional DC-DC stage in a two-stage design can filter twice-line-frequency ripple power. The drawback is additional loss from the extra power stage.

A variety of LED driving methods have been investigated to achieve flicker-free LED driving performance while maintaining high efficiency, low cost. Some focus on control strategy [4]-[6] while others focus on power topology [7]-[9] and [10]-[15]. One important research on LED drivers is eliminating electrolytic capacitors. Electrolytic capacitors are often used as high-density energy storage device, buffering the twice-line-frequency imbalanced energy. However, it compromises system life. Like any other semiconductor devices, LEDs can last for decades. On the other side, the lifespan of electrolytic capacitors is an order of magnitude less [16]. Therefore, eliminating them in LED driver designs becomes paramount. A few electrolytic capacitor LED drivers had been proposed in previous research [17]-[20].

A cycle by cycle current energy buffering Flyback LED driver has been proposed in this paper. The method treats imbalanced energy at switching frequency level, resulting in the following benefits as compared to previous electrolytic capacitor-less LED driver: (1) The imbalanced energy experiences one less time circulation in the system. (2) The maximum energy that needs to be stored in the main Flyback transformer, in every switching cycle, is half the amount that of conventional designs and other three- port LED drivers. (3) Primary side control can be easily implemented with the proposed LED driver.

The remaining part of this paper is organized as follows. The operating principle of the proposed LED

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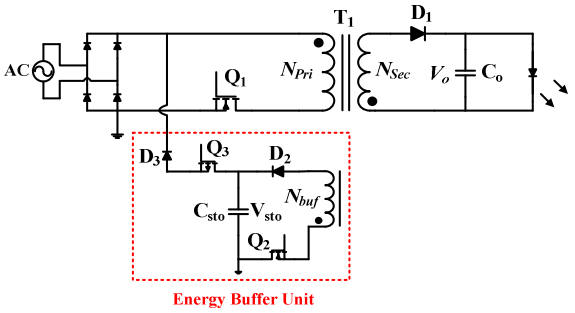


Fig. 1 The proposed cycle by cycle energy buffering LED driver

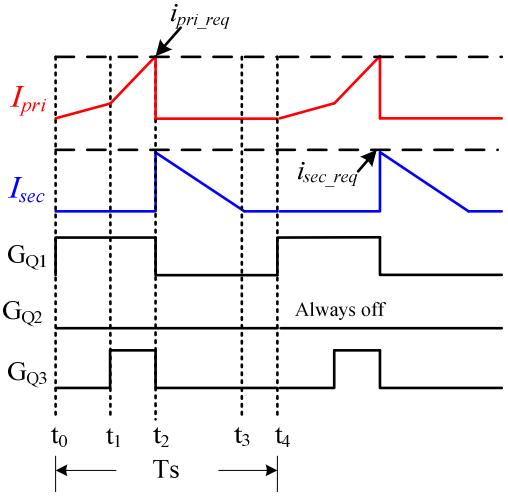


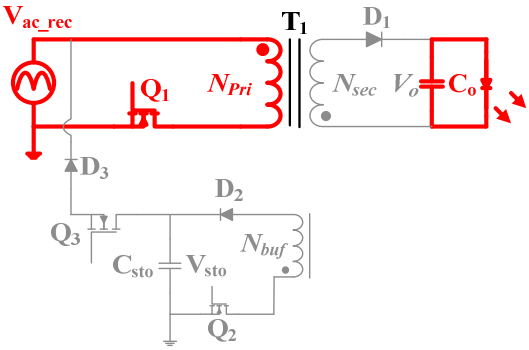
Fig. 2 Key switching waveforms of the proposed LED driver when Pin < PLED

driver is discussed in section II and the control strategy is discussed in section III. The experimental result is presented in Section IV and the paper is concluded in Section V.

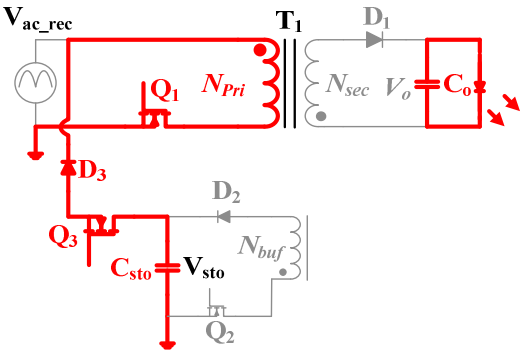
II Operating Principle

The proposed LED driver is shown in Fig. 1. The power stage is based on the Flyback topology with an extra energy buffering unit (EBU) to achieve high power factor and constant current output in every switching cycle. When $P_{in} < P_{LED}$, the additional energy is supplied from the storage capacitor, C_{sto}, to the LED load. When $P_{in} > P_{LED}$, the extra energy is stored into C_{sto}. The output capacitor C_o is implemented by a 10μF ceramic capacitor in the experimental prototype to filter the switching frequency ripple. The storage capacitor, C_{sto}, is implemented with a 2 x 3.3μF, 450V film capacitor. The switching operations during $P_{in} < P_{LED}$ and $P_{in} > P_{LED}$ are different and they will be discussed separately.

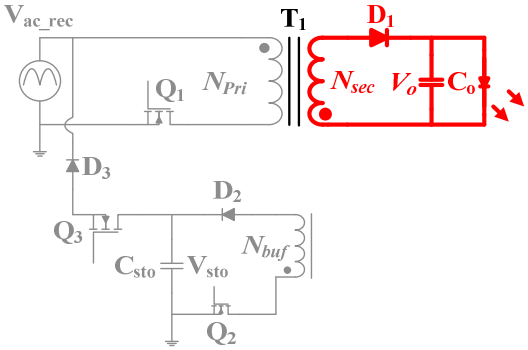
A. Operation when $P_{in} < P_{LED}$



(a) During [t_0-t_1]



(b) During [t_1-t_2]



(c) During [t_2-t_3]

Fig. 3 Switching operation when $P_{in} < P_{LED}$

The LED driver is operated under discontinues conduction mode (DCM) with four distinct time intervals, [t_0-t_1], [t_1-t_2], [t_2-t_3], [t_3-t_4] in one switching cycle. The critical switching waveforms are shown in Fig. 2.

During [t_0-t_1]

Fig. 3(a) illustrates the circuit operation during the time interval [t_0-t_1] when $P_{in} < P_{LED}$. The MOSFET Q_1 is turned on at t_0 and current is drawn from the AC input.

Because the primary side winding, $N_{pri,}$ is oriented in Flyback mode with respect to the secondary side windings, N_{sec}, and buffer winding, N_{buf}, the diode D_1, D_2 are reverse biased. This interval ends at time t_1 when the switching current drawn from the AC input reaches the level required for power factor correction.

During [t_1-t_2]

Fig. 3(b) illustrates the circuit operation during the time interval [t_1-t_2]. The MOSFET Q_3 is turned on at t_1 and Q_1 is remaining on. Because V_{sto} is higher than V_{in_rec}, the input bridge rectifier is reversed biased, and there is no more current drawn from the AC input during this time interval. C_{sto} provides the switching current in primary side winding instead. No AC input current during [t_1-t_2] is desirable as enough AC current had been drawn for power factor correction during [t_0-t_1]. D_1 and D_2 are still reverse biased, and Q_2 is forward biased. This time interval ends at time t_2 when the primary side switching current hits I_{pri_req}, which represents the current level required for delivering a constant LED output current. I_{pri_req} is automatically generated by a feedback loop that will be discussed in Section V. Both Q_1 and Q_3 are turned off at t_2.

During [t_2-t_3]

Fig. 3 (c) illustrates the circuit operation during the time interval [t2-t3]. As Q_1, Q_3 are turned off at t_2 and Q_2 is still off, the magnetic current is forced to commute from the winding N_{pri} to the winding N_{sec}. The voltage on the secondary side winding is clamped at Vo with ignoring the forward voltage drop on D1. The voltage on the secondary side winding is reflected to the primary side winding and the buffer winding. The magnetic current in winding N_{sec} starts decreasing at t_2 and becomes zero at t3, which ends this time interval.

B. Operation when $P_{in} > P_{LED}$

When $P_{in} > P_{LED}$, the extra energy is transferred from the AC input to the storage capacitor C_{sto} in every switching cycle. Fig. 4 shows the key switching waveforms with one switching cycle being divided into five time intervals, [t'_0-t'_1], [t'_1-t'_2], [t'_2-t'_3], [t'_3-t'_4] and [t'_4-t'_5].

During [t'_0-t'_1]

Fig. 5(a) shows the circuit operation during the time

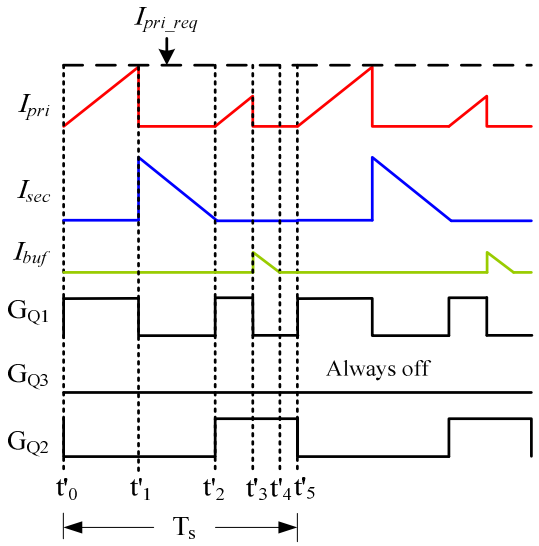


Fig. 4 Key switching waveforms of the proposed LED driver when $P_{in} > P_{LED}$

interval [t'_0-t'_1] when $P_{in} > P_{LED}$. It is the same as Fig. 3 (a) when $P_{in} < P_{LED}$. At t'_1, the primary side winding reaches I_{pri_req} and Q_1 is turned off. One should note that the current drawn from the AC input is not enough required by performing power factor correction yet at t_1. More current will be drawn from AC input during the time interval [t'_2-t'_3].

During [t'_1-t'_2]

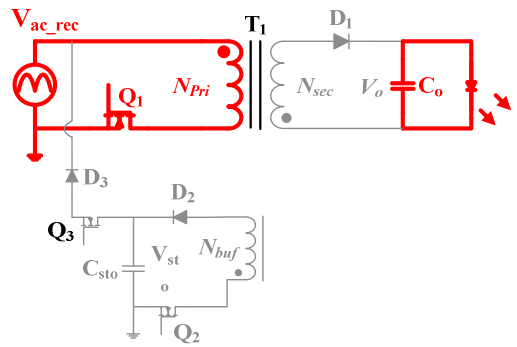
Fig. 5(b) shows the circuit operation during the time interval [t'_1-t'_2] when $P_{in} > P_{LED.}$ It is the same as Fig. 3 (b). This interval ends at t_2 when the secondary side current drops to zero.

During [t'_2-t'_3]

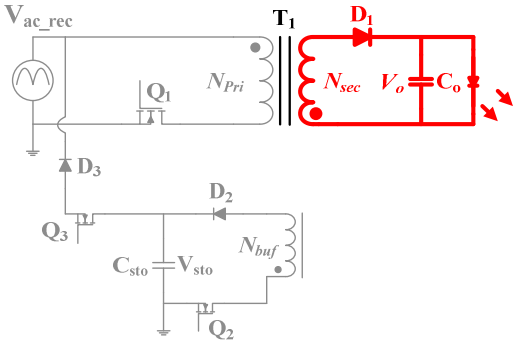
Fig. 5(c) shows the circuit operation during the time interval [t_2-t_3] when $P_{in} > P_{LED.}$ Q_1 is turned on again at t_2 to draw more current from AC input. This time interval ends at t_3 when the exact amount of current required for power factor correction is drawn from AC input.

During [t'_3-t'_4]

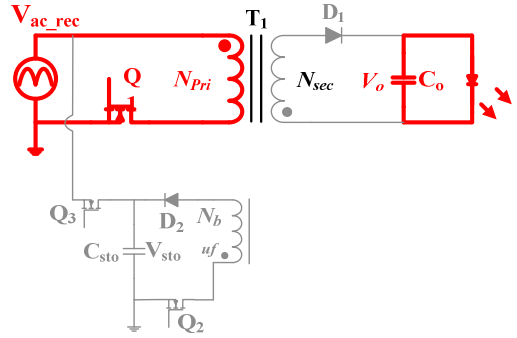
Fig. 5(d) shows the circuit operation during the time interval [t_3-t_4] when $P_{in} > P_{LED.}$ Since Q_1 is turned off at t_4 and the Q_2 is already on, the magnetic current commutes from winding N_{pri} to winding N_{buf}. The magnetic current does not flow in secondary side winding because of the following relationship in the design:



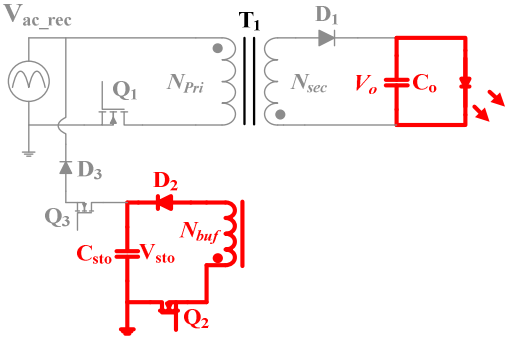
(a) During [t_0-t_1]



(b) During [t_1-t_2]



(c) During [t_2-t_3]



(d) During [t_3-t_4]

Fig. 5 Switching operation when $P_{in} > P_{LED}$

$$Vsto \div \left(\frac{Nsec}{Nbuf}\right) < Vo \qquad (1)$$

When the magnetic current flows in winding N_{buf}, the voltage on the winding is clamped at V_{sto}. The term on the left side of (1) is equal to the voltage reflected to the secondary side winding at the time. Therefore, the LED output voltage during [t'_3-t'_4] is higher than the secondary side winding voltage and the diode D_1 is reverse biased to block current. This time interval ends at t_4 when the magnetic current in winding N_{buf} decreases to zero.

C. Overall operation in a half line cycle

Since the switching operations, under both $P_{in}<P_{LED}$ and $P_{in}>$PLED, have been discussed, the overall view of the operation in a half line cycle is illustrated in Fig. 6.

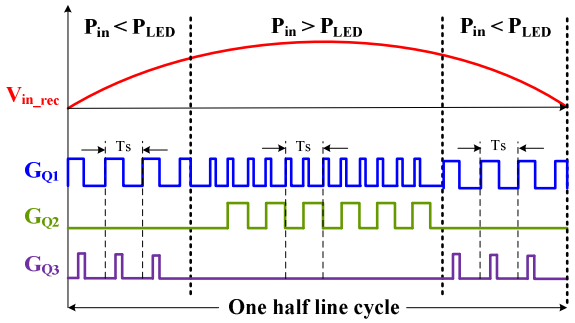


Fig. 6 Switching operation over a half line cycle

The above discussion also reveals that the imbalanced energy had only gone through two times power conversion. When $P_{in}> P_{LED}$, the imbalanced energy is transferred from AC input side to the storage capacitor, directly. When $P_{in} < P_{LED}$, it is then transferred from energy storage capacitor to LED output side. One less time power conversion had been achieved with the proposed LED driver as compared to active filter and previous three-port LED drivers.

III CONTROL STRATEGY

Fig. 7 (a) shows the control diagram of the proposed energy buffering LED driver and Fig. 7(b) & (c) give the example gate driving logic for both $P_{in} > P_{LED}$ and $P_{in} < P_{LED}$. There are two control loops, LED current loop and V_{sto} voltage loop in the system.

In the LED current loop, the LED current is sensed and compared with the reference, I_{LED_ref}. The compensated error, I_{pri_req}, becomes the boundary of the primary side

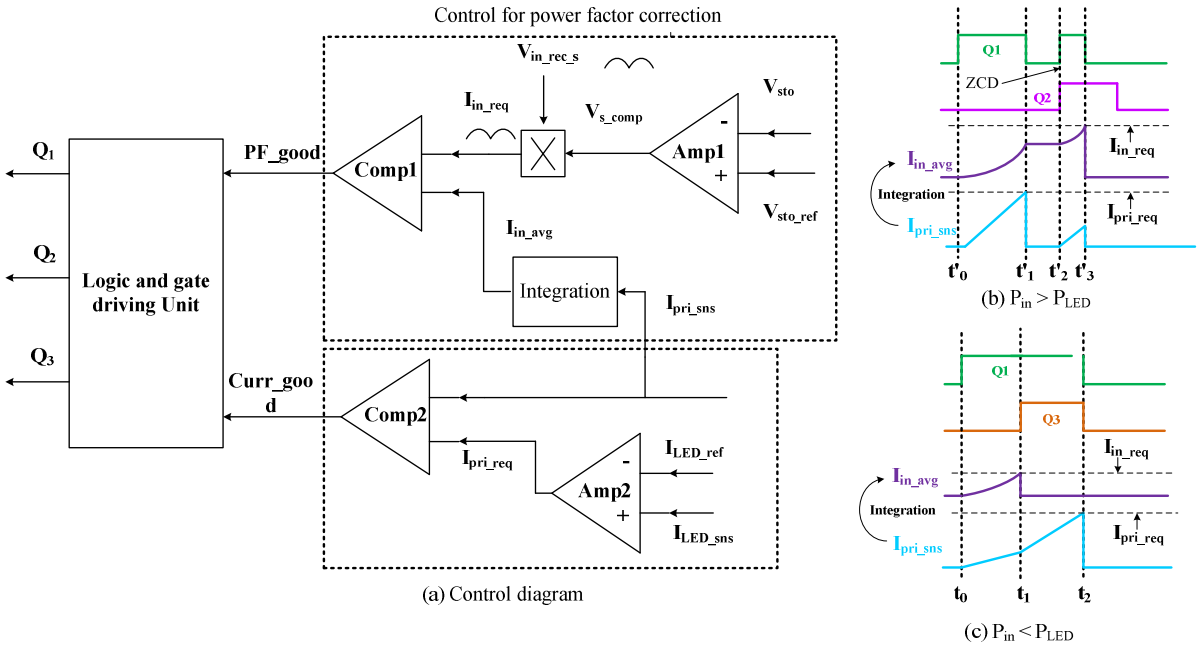


Fig. 7 Control scheme of the proposed LED driver

switching current. The sensed primary side switching current, I_{pri_sns} is compared with I_{pri_req}. Once I_{pri_sns} hits I_{pri_req}, no more current will be drawn from the primary side. Thus, the peak secondary side switching current is the same in every switching cycle to achieve constant LED output current. The current feedback loop determines the peak primary (also secondary) side current to achieve LED current regulation.

In the V_{sto} voltage loop, the averaged voltage of V_{sto}, V_{sto_avg}, is compared with its reference, V_{sto_ref}. The compensated error, V_{s_comp} multiples the scaled input voltage, $V_{in\_rec\_s}$, and the result becomes the reference of the AC input current. The average input current is obtained by taking I_{pri_sns}, for integration in every switching cycle. The result, I_{in_avg}, is compared with I_{in_ref}. Once I_{in_avg} hits I_{in_ref}, no more current will be drawn from AC input. Therefore, the function of power factor correction is achieved. The voltage feedback loop determines the AC input current to achieve V_{sto_avg} regulation.

Fig. 7 (b) illustrates the corresponding gate driving signal when $P_{in} > P_{LED}$. At time t_0, Q_1 is turned on. I_{in_avg} is the integrated result of I_{pri_sns}. I_{pri_sns} hits I_{pri_req} at time t_1 while I_{in_avg} is still lower than I_{in_ref}. The control system identifies $P_{in}>P_{LED}$. Q_1 is turned off at time t_1 and magnetic current commutes from primary side to secondary side. At time t_2, the secondary side current drops to zero and generates a signal ZCD. During $[t_1\text{-}t_2]$, I_{in_avg} is constant as there is no current from AC input. Q_1 is turned on again at t_2 and I_{pri_sns} starts rising from zero. Q_2 is also turned on at t_2. I_{in_avg} continues increasing until t_3, when I_{in_avg} hits I_{in_ref}. Q_1 is turned off at t_3 while Q_2 remains on. The magnetic current commutes from primary side to auxiliary side.

Fig. 7 (c) illustrate the corresponding gate driving signals when $P_{in} < P_{LED}$. At time t_0, Q_1 is turned on. I_{in_avg} is the integrated result of I_{pri_sns}. I_{in_avg} hits I_{in_ref} at t_1 while I_{pri_sns} is still lower than I_{pri_req}. The control system identifies $P_{in} < P_{LED}$. Therefore, Q_3 is turned on at t_2 and no more current will be drawn from AC input. The primary side switching current keeps increasing until t_3, when I_{pri_sns} hits I_{pri_req}. Both Q_1 and Q_3 are turned off then and the switching current commutes to secondary side.

It is worth to mention that the proposed LED driving method enables primary side current regulation. Under steady state, the peak secondary side current in every switching cycle is a constant. The secondary side current conduction time, which corresponds to $(t_2\text{-}t_1)$ in Fig. 2 and $(t'_3\text{-}t'_2)$ in Fig. 4, can be sensed by detecting winding voltages. Therefore, the averaged secondary side current in one switching cycle can be expressed as:

$$I_{LED} = \frac{I_{sec\_pk} \times T_{dis}}{2 \times T_s} \quad (1)$$

Where T_{dis} is equal to $(t_2\text{-}t_1)$ in Fig. 2 and $(t'_3\text{-}t'_2)$ in Fig. 4. The peak secondary side current and the peak primary side current has the following relationship:

$$I_{pri\_pk} = I_{sec\_pk} \times \frac{N_{sec}}{N_{pri}} \quad (2)$$

The peak primary side current is also equal to the control signal I_{pri_req}. Therefore, the averaged LED current can be rewritten as:

$$I_{LED} = \frac{I_{Pri\_req} \times T_{dis} \times N_{pri}}{2 \times T_s \times N_{sec}} \quad (3)$$

Once I_{pri_req} and T_{dis} are sensed, the LED current can be estimated without additional sensing on the secondary side. [21] and [22] have the details of primary side circuit sensing technology and will not be further discussed in this paper.

IV EXPERIMENTAL RESULT

To verify the operating principle of the proposed LED driver, a 15W experimental prototype had been built and tested. The circuit parameter is shown in TABLE 1.

TABLE 1 The experimental prototype specification and key components

System Specification	
Input voltage	89Vrms – 132Vrms
Maximum output voltage	~60V
Maximum output current	0.25A
Maximum output power	15W
Circuit Parameter	
Transformer	N_{pri}: N_{sec}: N_{buf} = 3:1:3 L_{pri}=1.2mH, EE16 core
Switching frequency	25KHz
Controller	dsPIC33FJ32GS606
MOSFET Q1	STP5N60M2, 600V, 3.7A
MOSFET Q2, Q3	FQP3N30, 300V, 3.2A
Diode D1, D2, D3	LQA03TC600, 600V, 3A
Output capacitor	CGA9N3X7S2A106K230KB, 100V, 10μF
Storage capacitor	2 x ECW-FD2W335K 450V, 3.3μF

Fig. 8 shows the key switching waveforms when $P_{in} < P_{LED}$. Fig. 9 shows the key switching waveforms when $P_{in} > P_{LED}$. Fig. 10 shows the key waveforms of line frequency operation, which includes the AC input current, the LED voltage, the LED current and the storage capacitor voltage Vsto. The LED voltage is almost a constant. FFT function is used to measure 120Hz ripple LED current to avoid misreading due to switching noise. The RMS ripple LED current at 120Hz is 10.67mA, which corresponds to 15mA peak ripple and is 6% of the average LED current. The voltage on storage capacitor, V_{sto}, changes from 120V as the minimum to 170V as the maximum in a half line cycle, to buffer the imbalanced energy.

Fig. 11 compares the efficiency of the proposed LED driver and a comparable conventional single-stage LED driver. At full load, the efficiency of the proposed LED driver is only 1.2% lower than the efficiency of a conventional Flyback LED driver, which is a very small price to pay when flicker-free and electrolytic capacitor free operation have been achieved. Fig. 12 shows the power factor of the proposed LED driver. At full load, the experimental prototype achieves 0.94PF, which meets the requirement from EnergyStar.

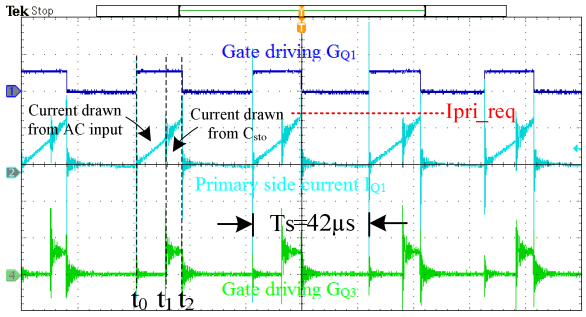


Fig. 8 Key switching waveforms when $P_{in} < P_{LED}$

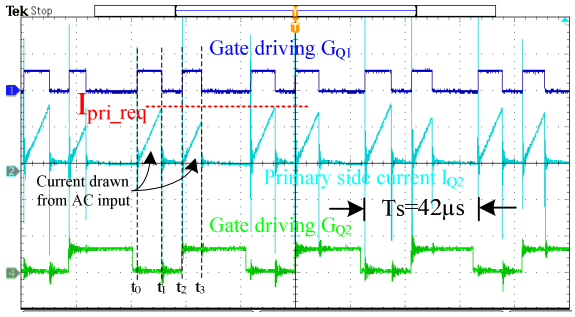


Fig. 9 Key switching waveforms when Pin > PLED

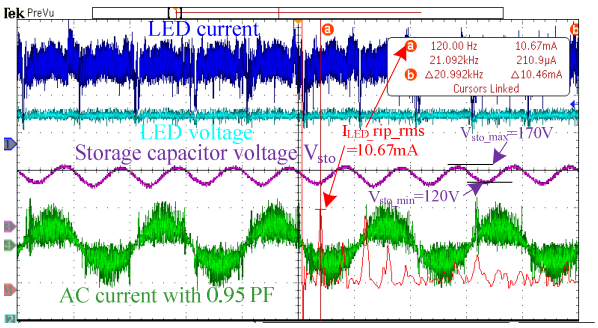


Fig. 10 Key waveforms in twice line frequency operation

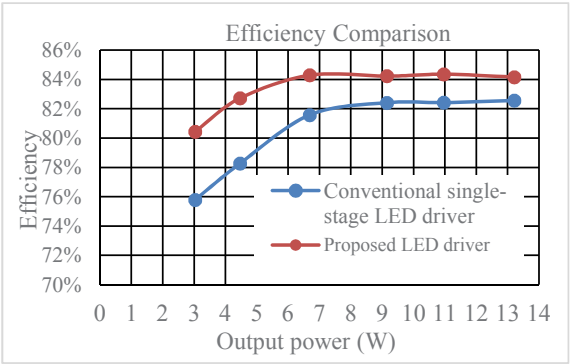


Fig. 11 Efficiency comparison

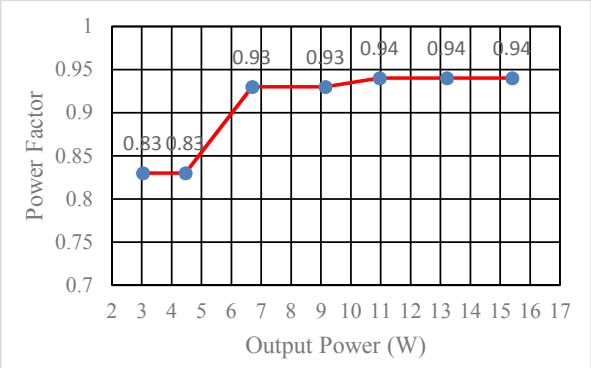


Fig. 12 Power factor performance under 110Vrms input, full load

V CONCLUSION

Eliminating electrolytic capacitors in LED driver design is critical to expand the lifetime of LED lighting fixtures. A cycle by cycle energy buffering LED driver has been proposed in the paper to achieve electrolytic-less and flicker-free operation. A 15W experimental prototype had been built and tested to verify the operating principle. 0.94PF has been achieved. The efficiency of the proposed LED driver is only 1.5% lower than a conventional single-stage LED driver at full load, which is a low price to pay when achieving flicker-free operation and electrolytic capacitor-less design. The 120Hz ripple current is measured to be 6% of the average LED current. Overall, the experimental result shows a high degree of agreement with the analysis and it is very satisfying.

REFERENCES

[1] ENERGY STAR Program Requirements for Solid State Lighting Luminaires, Version 1.1, December 19, 2008.

[2] B. Lehman, A. Wilkins, S. Berman, M. Poplawski and N. J.Miller, "Proposing measures of flicker in the low frequencies for lighting applications," in *Energy Conversion Congress and Exposition*, Phoenix, AZ, Sept 2011.

[3] X.B. Ruan, B.B. Wang, K. Yao and S. Wang, "Optimum Injected Current Harmonics to Minimize Peak-to-Average Ratio of LED Current for Electrolytic Capacitor Less AC–DC Drivers" in *IEEE Transactions on Power Electronics*, Vol. 26, No. 7, pp.1820-1825, July 2011.

[4] G. G. Pereira, M. A. Dalla Costa, J. M. Alonso, M. F. De Melo and C. H. Barriquello, "LED Driver Based on Input Current Shaper Without Electrolytic Capacitor," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4520-4529, June 2017.

[5] D. G. Lamar, J. Sebastian, M. Arias and A. Fernandez, "On the Limit of the Output Capacitor Reduction in Power-Factor Correctors by Distorting the Line Input Current," in *IEEE Transactions on Power Electronics*, Vol. 27, No. 3, pp. 1168-1176, March 2012.

[6] F.H. Zhang, J.J.Ni and Y.J.Yu, "High Power Factor AC–DC LED Driver With Film Capacitors," in *IEEE Transactions on Power Electronics*, Vol. 28, No. 10, pp. 4831-4840, October 2013.

[7] C.A. Cheng, C.H. Chang, T.Y. Chung and F.L. Yang, "Design and Implementation of a Single-Stage Driver for Supplying an LED Street-Lighting Module with Power Factor Corrections," in *IEEE Transactions on Power Electronics*, Vol. 30, No. 2, pp. 956-966, February 2015.

[8] J. C. W. Lam and P. K. Jain, "Isolated AC/DC Offline High Power Factor Single-Switch LED Drivers Without Electrolytic Capacitors," in IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 3, No. 3, pp. 679-690, September 2015.

[9] J. C. W. Lam and P. K. Jain, "A High Power Factor, Electrolytic Capacitor-Less AC-Input LED Driver Topology with High Frequency Pulsating Output

Current," in IEEE Transactions on Power Electronics, Vol. 30, Vo. 2, pp. 943-955, February 2015.

[10] H. Ma, J. S. (. Lai, C. Zheng and P. Sun, "A High-Efficiency Quasi-Single-Stage Bridgeless Electrolytic Capacitor-Free High-Power AC–DC Driver for Supplying Multiple LED Strings in Parallel," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5825-5836, Aug. 2016.

[11] P. Fang, Y. F. Liu and P. C. Sen, "A Flicker-Free Single-Stage Offline LED Driver With High Power Factor," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 654-665, Sept. 2015.

[12] P. Fang, Y. j. Qiu, H. Wang and Y. F. Liu, "A Single-Stage Primary-Side-Controlled Off-line Flyback LED Driver With Ripple Cancellation," in IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4700-4715, June 2017.

[13] P. Fang and Y. F. Liu, "Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation with True Single Stage Power Factor Correction," in IEEE Transactions on Power Electronics, vol. 32, no. 5, pp. 3892-3907, May 2017.

[14] Y. Qiu, L. Wang, H. Wang, Y. F. Liu and P. C. Sen, "Bipolar Ripple Cancellation Method to Achieve Single-Stage Electrolytic-Capacitor-Less High-Power LED Driver," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 3, pp. 698-713, Sept. 2015.

[15] D.Camponogara, G.F.Ferreira, A. Campos, M.A. Dalla Costa and J. Garcia, "Offline LED Driver for Street Lighting with an Optimized Cascade Structure," in IEEE Transactions on Industry Applications, Vol.49, No 6, pp.2437-2443, December 2013.

[16] E. Rifa, “Electrolytic capacitors application guide,” Appl. Note, Evox Rifa AB, Gr¨anna, Sweden, 2001.

[17] Q.C. Hu and R. Zane, "Minimizing Required Energy Storage in Off-Line LED Drivers Based on Series-Input Converter Modules," in IEEE Transactions on Power Electronics, Vol. 26, No. 10, pp.2887-2895, October 2011.

[18] S. Wang, X.B. Ruan, K. Yao, S.C. Tan, Y. Yang and Z.H. Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver" in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp.4540-4548, November 2012.

[19] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou and E. C. Tatakis, "Investigation of Parallel Active Filters’ Limitations for Power Decoupling on Single-Stage/Single-Phase Microinverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1096-1106, Sept. 2016.

[20] W. Chen and S.Y.R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver with High Input Power Factor and Constant Output Current," in IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1598-1607, March 2012.

[21] Y.C. Li and C.L. Chen, "A Novel Primary-Side Regulation Scheme for Single-Stage High-Power-Factor AC–DC LED Driving Circuit," in IEEE Transactions on Industrial Electronics, Vol. 60, No. 11, pp.4978-4986, November 2013.

[22] X.G. Xie, J. Wang, C. Zhao, Q. Lu and S.R. Liu, "A Novel Output Current Estimation and Regulation Circuit for Primary Side Controlled High Power Factor Single-Stage Flyback LED Driver," in IEEE Transactions on Power Electronics, Vol. 27, No. 11, pp. 4602-4612, November 2012.